IN THE CLAIMS

1. (Original) A computer system comprising:

a system controller including a central processing unit and a memory bus controller and configured to operate in a first interface mode;

a system memory connected with the system controller through the system bus;

a NAND flash memory configured to store a system driving code, an operating system program, and user data for the computer system; and

an interface unit configured to communicate with the system controller through the system bus in the first interface mode and configured to communicate with the NAND flash memory in a second interface mode, the interface unit being synchronized with a clock signal generated in response to predetermined command information.

2. (Original) The computer system of claim 1, wherein the interface unit comprises:

a host interface unit configured to communicate with the system controller through the system bus in the first interface mode;

a register unit configured to store configuration information about the computer system, the NAND flash memory, and the command information;

a buffer unit for configured to store data of the NAND flash memory;

an oscillator configured to generate the clock signal in response to the command information;

a state machine synchronized with the clock signal and configured to control an inner operation of the interface unit in response to the command information; and

a NAND flash interface unit synchronized with the clock signal and configured to communicate with the NAND flash memory via the state machine in the second interface mode.

3. (Original) The computer system of claim 2, wherein the interface unit further comprises a power-up detector configured to apply a power sensing signal to the state machine when power is applied.

4. (Original) The computer system of claim 3, wherein the interface unit further comprises an error correcting circuit synchronized with the clock signal and configured to perform an error test and correction on the data of the NAND flash memory.

5. (Original) The computer system of claim 4, wherein the state machine comprises:

a first block configured to control operations to program the data stored in the buffer unit and predefined error correcting parity bits in the NAND flash memory;

a second block configured to control an operation to store the data read out of the NAND flash memory in the buffer unit;

a third block configured to control an operation to boot the compute system by using the system bootstrap code stored in the NAND flash memory; and

a fourth block configured to control an operation to generate the error correcting parity bits during the programming operation of the NAND flash memory and configured to control an operation to correct an error by comparing the parity bits stored in the NAND flash memory with new parity bits during the read operation of the NAND flash memory.

6. (Original) The computer system of claim 5, wherein the state machine further comprises:

a fifth block configured to control an operation to erase the data stored in the NAND flash memory; and

a sixth block configured to apply a reset command to the NAND flash memory and to a plurality of registers within the interface unit.

7. (Original) The computer system of claim 1, wherein the interface unit comprises:

a first interface unit configured to communicate with the system controller through the system bus in the first interface mode;

a second interface unit synchronized with the clock signal and configured to communicate with the NAND flash memory in the second interface mode;

a storage unit configured to store information and data exchanged between the first and second interface units; and

a control unit synchronized with the clock signal and configured to control a transmission of the information and data between the first and second interface units.

8. (Original) The computer system of claim 7, wherein the storage unit comprises:

a register unit configured to store configuration information about the computer system, the NAND flash memory, and the command information about the NAND flash memory; and

a buffer unit configured to store data of the NAND flash memory.

9. (Original) The computer system of claim 7, wherein the interface unit further comprises a power-up detector configured to apply a power sensing signal to the state machine when power is applied.

10. (Original) The computer system of claim 9, wherein the interface unit further comprises an error correcting circuit synchronized with the clock signal and configured to perform an error test and correction on the data of the NAND flash memory.

11. (Original) The computer system of claim 7, wherein the control unit comprises:

a first block configured to control operations to program the data stored in the buffer unit and predefined error correcting parity bits in the NAND flash memory;

a second block configured to control an operation to store the data read out of the NAND flash memory in the buffer unit;

a third block configured to control an operation to boot the compute system by using the system bootstrap code stored in the NAND flash memory; and

a fourth block configured to control an operation to generate the error correcting parity bits during the programming operation of the NAND flash memory and configured to control an operation to correct an error by comparing the parity bits stored in the NAND flash memory with new parity bits during the read operation of the NAND flash memory.

12. (Original) The computer system of claim 11, wherein the control unit further comprises:

a fifth block configured to control an operation to erase the data stored in the NAND flash memory; and

a sixth block configured to apply a reset command to the NAND flash memory and to a plurality of registers within the interface unit.

13. (Cancelled)

14. (Currently Amended) A method ~~for reading out data~~ of performing an interleaved read operation from a NAND flash memory in a computer system having a system controller and a buffer, the NAND flash memory having storage regions, each storage region consisting of a plurality of pages, the method comprising:

initializing the read operation by setting ~~commands, addresses, and~~ commands and addresses for selected pages to be read out from the NAND flash memory;

copying first data ~~of a first page from the NAND flash memory~~ from a first one of the selected pages to the buffer during a first time frame; ~~and~~

copying second data ~~of a second page from the NAND flash memory~~ from a second one of the selected pages to the buffer during a second time frame, copying second data including waiting over a latency period required for a read operation; and

~~while~~ transmitting the first ~~page~~ data from the buffer to the system controller during the second time frame.

15. (Original) The method of claim 14, further comprising:

copying data of a N^{th} page to the buffer from the NAND flash memory while transmitting data of a $(N-1)^{th}$ page until the copying of all the pages is completed.

16. (Original) The method of claim 14, wherein the data of the pages is transmitted successively.

17. (Currently Amended) A method ~~for programming data from~~ of performing an interleaved program operation to a NAND flash memory in a computer system ~~with~~ having a system controller and a buffer, the NAND flash memory having storage regions configured to store pages of data, the method comprising:

initializing the program operation by setting commands~~, addresses,~~ and addresses for the pages to be programmed to the NAND flash memory;

immediately after initializing, successively loading data necessary for the pages to be programmed from the system controller ~~to~~ into the buffer, where successively loading data means loading data into the buffer in the order in which the data is to be programmed to the NAND flash memory and that, except for the data for the last page to be programmed, no time delay exists between the loading of data for any one of the pages and the loading of data for a page to be programmed after the any one of the pages; and

sequentially programming the ~~pages~~ NAND flash memory by using the data loaded to the buffer, where the data for one of the pages is programmed to the NAND flash memory at the same time that the data for a page to be programmed immediately after the one of the pages is loaded into the buffer.

18. (Currently Amended) The method of claim 17, wherein the one of the pages is the first page to be programmed to the NAND flash memory ~~sequentially programming the pages comprises:~~

~~programming data the data for another page is being successively loaded to the buffer.~~